

#### US005911090A

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# **United States Patent** [19]

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[11]

### [54] PROCESS AND SYSTEM FOR FLATTENING SECONDARY EDGEBEADS ON RESIST COATED WAFERS

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#### Related U.S. Application Data

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[51] Int. Cl.<sup>6</sup> ...... G03D 5/00

134/157, 153, 198; 355/53, 43, 45; 430/311,

### [56] References Cited

**Patent Number:** 

#### U.S. PATENT DOCUMENTS

| 4,113,492 | 9/1978  | Sato et al 427/273    |
|-----------|---------|-----------------------|
| 4,510,176 | 4/1985  | Cuthbert 118/52       |
| 4,518,678 | 5/1985  | Allen 427/273         |
| 4,732,785 | 3/1988  | Brewer 427/240        |
| 4,838,289 | 6/1989  | Kottman et al 134/153 |
| 5,151,219 | 9/1992  | Salamy et al 430/331  |
| 5,426,017 | 6/1995  | Johnson 430/331       |
| 5,580,607 | 12/1996 | Takekuma et al 118/52 |
|           |         |                       |

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# [57] ABSTRACT

A method and system of flattening resist mounds formed during a wet edgebead operation. The wet edgebead operation is used to remove edgebeads formed when a resist material is deposited on a semiconductor wafer. Solvent is introduced to the semiconductor wafer at the area containing the resist mounds to soften them, and the semiconductor wafer is spun at a high speed to flatten the mounds.

## 21 Claims, 7 Drawing Sheets

